

HUBER et al.
10/759,253

IN THE ABSTRACT:

Kindly replace the originally filed Abstract with the attached replacement Abstract.

Respectfully Submitted,

A handwritten signature in black ink, appearing to read "Will H Bollman". The signature is written in a cursive, flowing style.

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ABSTRACT

Using at best a 2.5V nominal power supply, 3.3V technology can be used to implement a 5V tolerant open drain output buffer. High voltage and/or current tolerance is achieved with only the 2.5V power supply. A p-channel FET transistor is connected between a power supply and a node, which in turn is connected to a node between two series output FET transistors. The first transistor is connected between the **PAD** and node, and the second transistor is connected between the node and ground. The gate of the second transistor is driven from another node formed between a series string of a p-channel FET transistor and an n-channel FET transistor. The other side of the first transistor is connected to the power supply, and the other side of the second transistor is connected to ground. The gates of the transistors of the inverter are tied together and driven by an applied signal.

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